

REMARKS

Claims 13 and 15-27 are pending in the action, with claims 13, 21 and 22 being independent. Claims 13, 21 and 22 are amended. Applicant submits that the amended language thereof does not narrow the original scope of these claims. No new matter has been added.

Claims 13, 15, 17, 20-24 and 26-27 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over JP No. 411205043A to Irie in view of USP No. 5,548,840 to Heck, and further in view of USP No. 5,280,648 to Dobrovolny.

Claims 16 and 25 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Irie in view of Heck and Dobrovolny, and further in view of USP No. 6,057,714 to Andrys.

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Irie in view of Heck and Dobrovolny, and further in view of USP No. 5,678,224 to Murtojarvi.

The Applicant traverses these rejections. Reconsideration and allowance of the above-referenced application are respectfully requested in light of the following remarks.

Section 103(a) Rejections

Claims 13, 15, 17, 20-24 and 26-27 are rejected as allegedly being unpatentable over Irie in view of Heck, and further in view of Dobrovolny.

Claim 13, as amended, recites in part an interconnection circuitry that **turns off** a second transistor when a first local oscillator input signal is applied to a first transistor during a first high period and **a first low period**.

In the statement of rejection, the Examiner admits that the combination of Irie and Heck does not teach these features, and relies upon the LO source 40 of Dobrovolny to cure this deficiency (page 4, lines 1-7).

Applicant submits that Dobrovolny does not teach turning off transistor 26 when an oscillating signal is applied to transistor 22 during a low period of transistor 22. In Dobrovolny, transistor 22 and transistor 26 are alternately switched ON and OFF (3:20-25). For example, when an oscillating signal is applied to transistor 22 during a high period of transistor 22,

transistor 26 is OFF. However, when an oscillating signal is applied to transistor 22 during a low period of transistor 22, transistor 22 is turned OFF and transistor 26 is alternately turned ON. Dobrovoly does not teach turning OFF transistor 26 when the LO source 40 applies an oscillating signal to transistor 22 during a low period of transistor 22.

Claim 13, as amended, also recites in part an interconnection circuitry to turn off the first transistor when the second local oscillator input signal is applied to the second transistor during a second low period. Similarly, Dobrovoly does not teach turning OFF transistor 22 when the LO source 40 applies an oscillating signal to transistor 26 during a low period of transistor 26. Rather, when the LO source 40 applies an oscillating signal to transistor 26 during a low period of transistor 26, transistor 26 is turned OFF and transistor 22 is alternately turned ON.

Thus, for at least these reasons, Applicant submits that claim 13, as amended, is allowable over the combination of Irie, Heck and Dobrovoly. Claims 15-20 depend on claim 13, and also are submitted to be allowable for analogous reasons discussed with respect claim 13.

Claim 21 recites an interconnection circuitry coupling the plurality of transistors, the interconnection circuitry configured to turn off transistors other than one transistor at which a local oscillation input signal is received during a high period and a low period of the one transistor. However, as discussed *supra*, in Dobrovoly, transistor 22 and transistor 26 are alternately switched ON and OFF. When an oscillating signal is applied to transistor 22 during a high period of transistor 22, transistor 26 is OFF. However, when an oscillating signal is applied to transistor 22 during a low period of transistor 22, transistor 22 is turned OFF, causing transistor 26 to turn ON. Dobrovoly does not teach turning OFF transistor 26 even when an oscillating signal is applied to transistor 22 during a low of transistor 22.

Thus, for at least these reasons, Applicant submits that claim 21, as amended, is allowable over the combination of Irie, Heck and Dobrovoly. Claims 23-26 depend on claim 21, and also are submitted to be allowable for analogous reasons discussed with respect claim 21.

Claim 22, as amended, recites in part turning off the second transistor during the first high period and the first low period when the first local oscillator input signal is applied to the first transistor and turning off the first transistor during the second high period and the second

low period when the second local oscillator input signal is applied to the second transistor. As discussed *supra*, the combination of Irie, Heck and Dobrovlny does not teach these features. Thus, Applicant submits that claim 22, as amended, is allowable over the combination of Irie, Heck and Dobrovlny. Claim 27 depends on claim 22, and also is submitted to be allowable for analogous reasons discussed with respect claim 22.

Conclusion

The Applicant respectfully requests that all pending claims be allowed.

By responding in the foregoing remarks only to particular positions taken by the Examiner, the Applicant does not acquiesce with other positions that have not been explicitly addressed. In addition, Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.


For all of the reasons set forth above, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's representative at the telephone number shown below.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 06-1050 and please credit any excess fees to such deposit account.

Respectfully submitted,

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